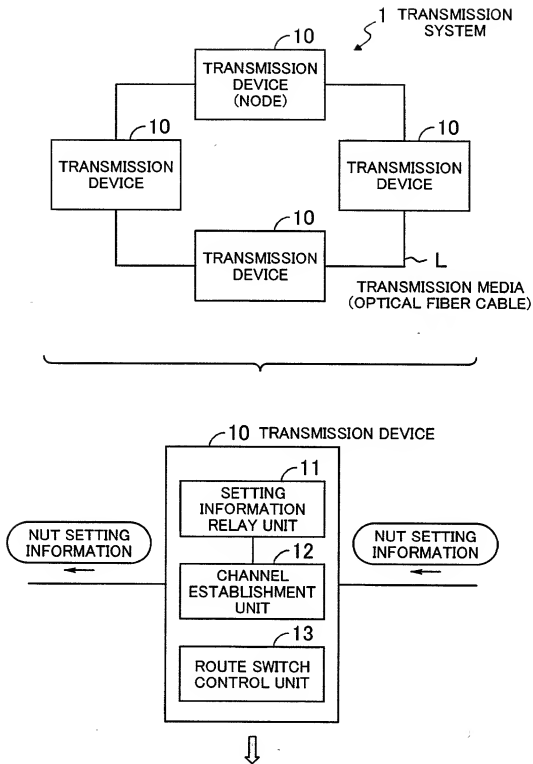


10090829 020502



EX. WHEN NUT SETTING IS GIVEN TO CH 25
FROM NUT SETTING INFORMATION, NUT OF
CH25 IS ESTABLISHED AND NUT RELAY
INFORMATION IS RELAYED.

FIG. 1

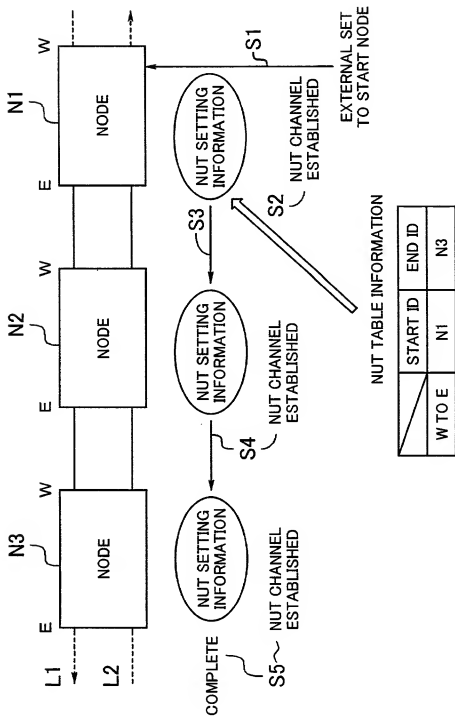


FIG. 2

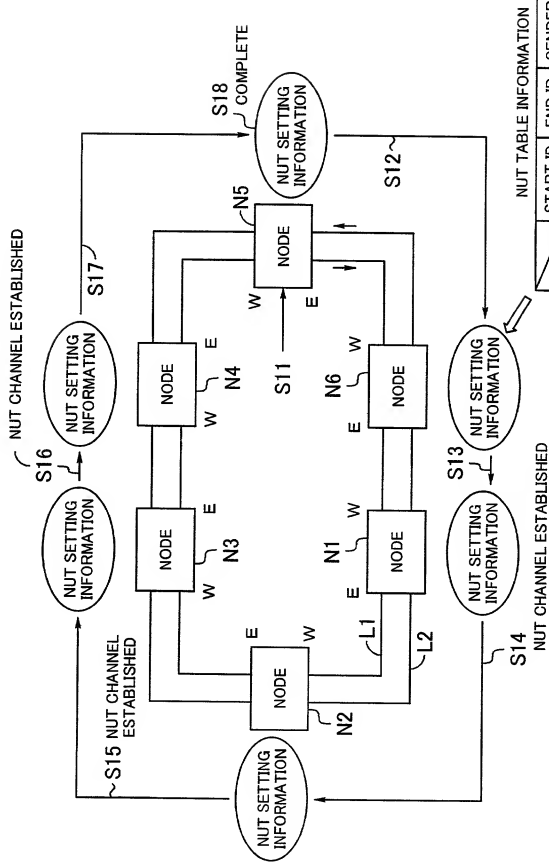


FIG. 3

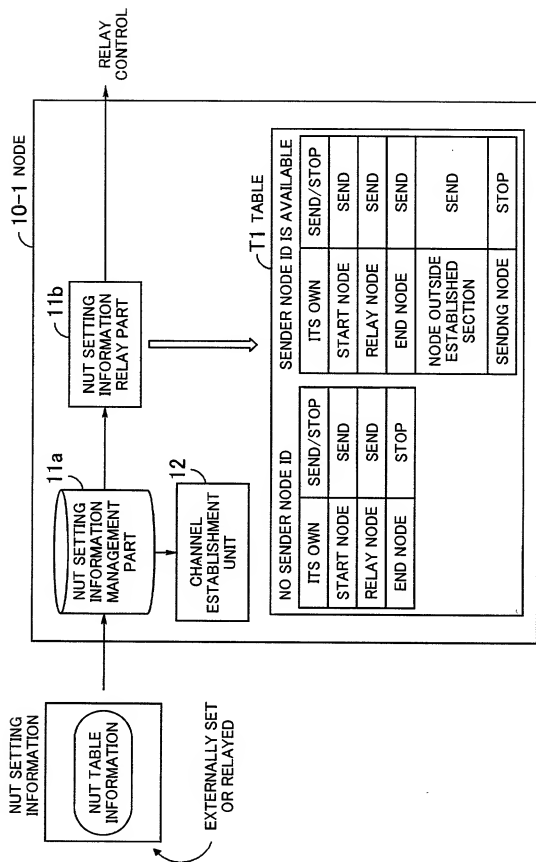


FIG. 4

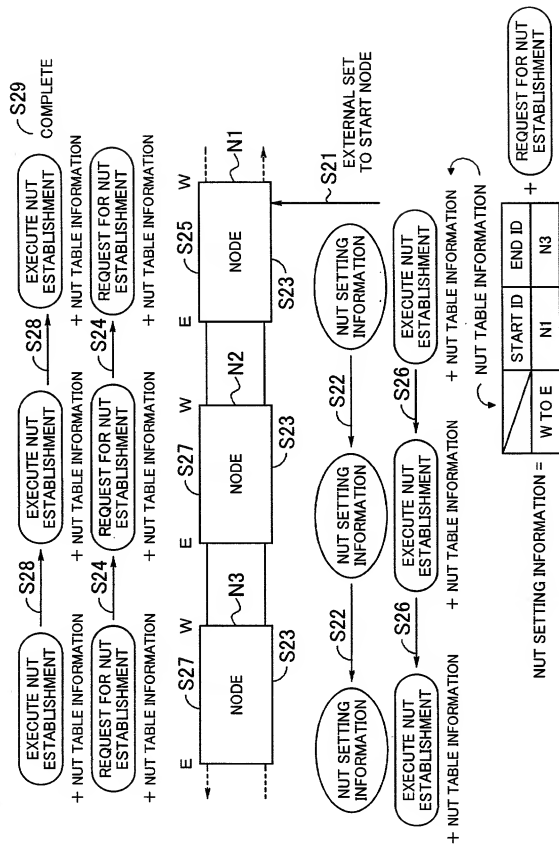


FIG. 5

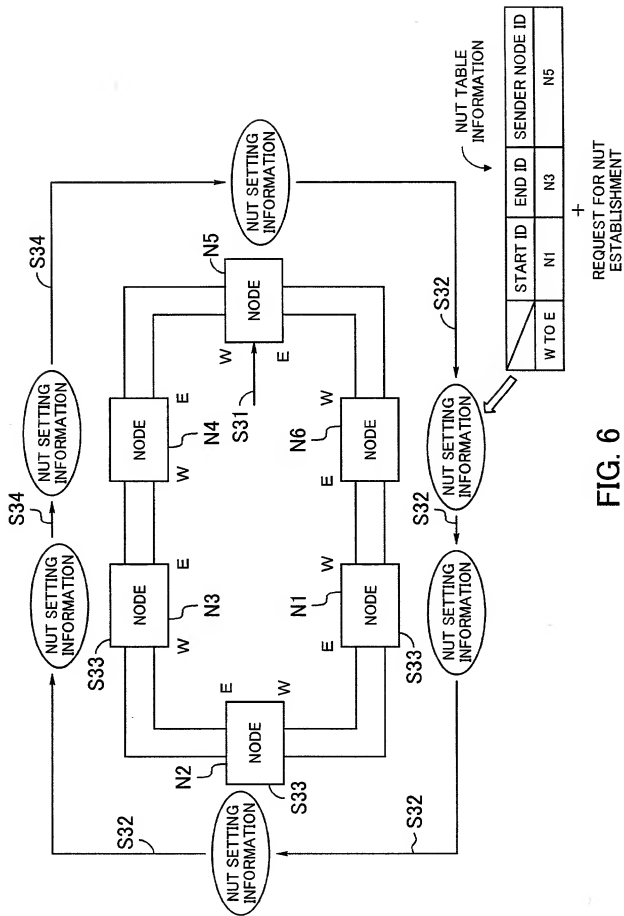
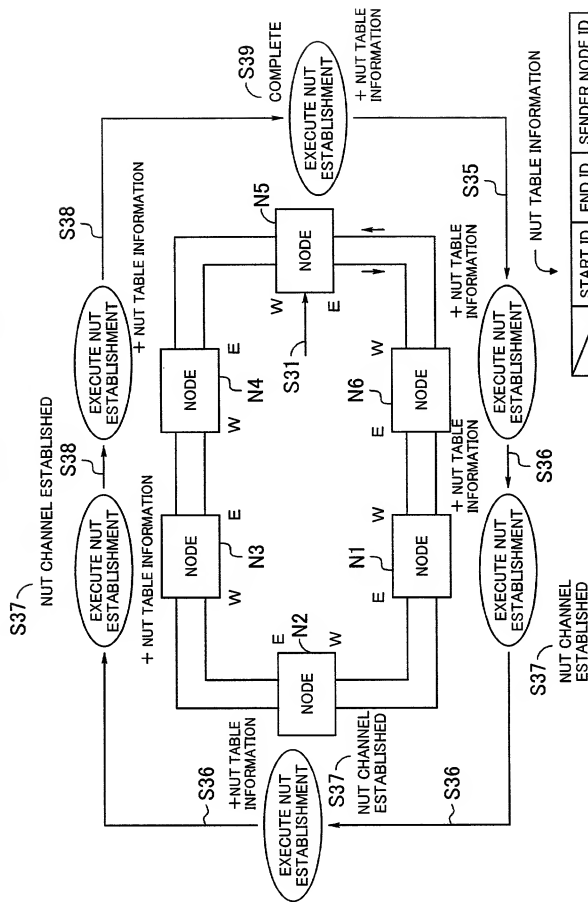


FIG. 6



START ID	END ID	SENDER NODE ID
N1	N3	N5

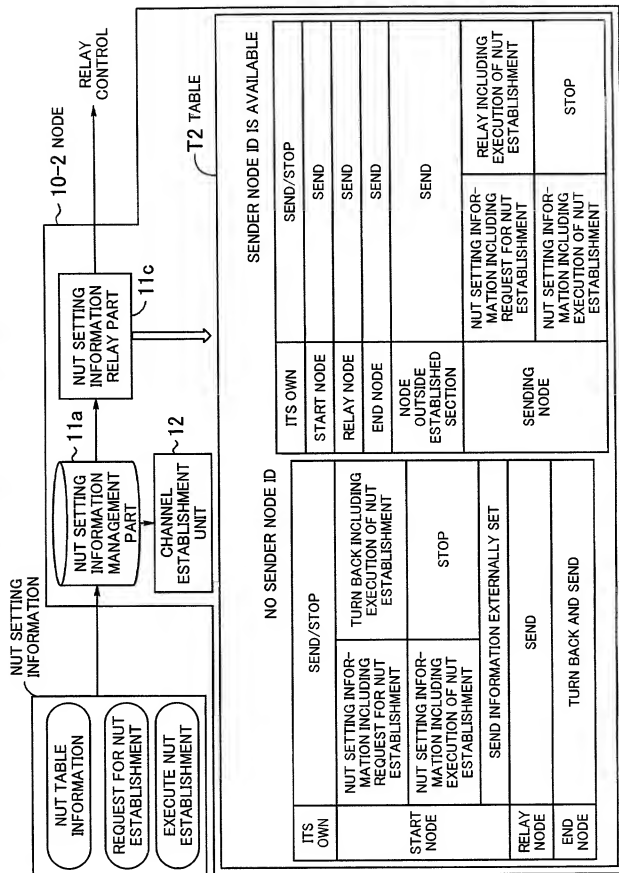


FIG. 8

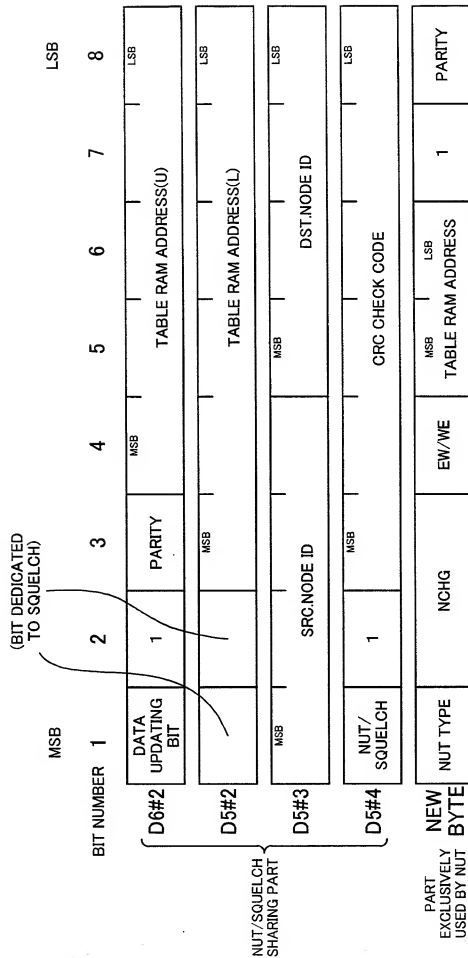


FIG. 9

D6#2 BYTE

BIT NO.

- 1: BIT INDICATING THAT DATA IS BEING UPDATED
- 2: FIXED TO "1"
- 3: ODD PARITY BIT FOR BITS 4-8
- 4-8: 5 UPPER BITS OF SQUELCH TABLE AND NUT TABLE RAM.
THESE BITS INDICATE ADDRESS OF NUT TABLE RAM TOGETHER WITH BITS 4-8 OF D6#2

{
"0" WRITING BY CPU IS INHIBITED
"1" WRITING BY CPU IS ALLOWED

D5#2 BYTE

BIT NO.

- 1: PART EXCLUSIVELY USED BY SQUELCH TABLE
- 2: PART EXCLUSIVELY USED BY SQUELCH TABLE
- 3-8: SIX LOWER BIT OF ADDRESS OF SQUELCH TABLE AND NUT TABLE RAM
THESE BITS INDICATE ADDRESS OF NUT TABLE RAM TOGETHER WITH BITS 4-8 OF D6#2

FIG. 10

D5#3 BYTE

BIT NO.

1-4: SRC.NODE ID (START NODE ID)

5-8: DST.NODE ID (END NODE ID)

D5#4 BYTE

BIT NO.

1: BIT INDICATING TYPE OF INFORMATION TO BE TRANSFERRED

1: SQUELCH TABLE

0: NUT SETTING INFORMATION

2: FIXED TO "1"

3-8: CRC6 Check code (BITS SUBJECTED TO CALCULATION: BITS 3-8 OF D5#2
BITS 1-8 OF D5#3)

FIG. 11

NEW BYTE

BIT NO.

1: BIT INDICATING TYPE OF NUT

1: BASIC NUT

0: ENHANCED NUT

2-3: BIT INDICATING NUT TABLE TRANSFER CONDITION

00: NUT SETTING RELEASE CONDITION

01: NUT SETTING RELEASE REQUEST CONDITION

10: NUT SETTING ESTABLISHMENT CONDITION

11: NUT SETTING ESTABLISHMENT REQUEST CONDITION

4: BIT INDICATING RELAY DIRECTION

1: EAST TO WEST (EW)

0: WEST TO EAST (WE)

5-6: GROUP IDENTIFIER, OC192 IS DIVIDED INTO FOUR GROUPS

7: FIXED TO "1"

8: ODD PARITY BIT FOR BITS 1-6

FIG. 12

10090939-0305002

T3

GROUP	RAM	SPAN	CH-NO.	ADD/DROP
0	000	1	1	ADD
0	001	1	1	DROP
0	002	1	2	ADD
0	003	1	2	DROP
0	004	1	3	ADD
0	005	1	3	DROP
----	----	----	----	----
0	05E	1	48	ADD
0	05F	1	48	DROP
0	060	2	1	ADD
0	061	2	1	DROP
----	----	----	----	----
0	0BE	2	48	ADD
0	0BF	2	48	DROP
----	----	----	----	----
0	5A0	16	1	ADD
0	5A1	16	1	DROP
----	----	----	----	----
0	5FE	16	48	ADD
0	5FF	16	48	DROP

↓
①

FIG. 13

①



↪ T3

GROUP	RAM	SPAN	CH-NO.	ADD/DROP
1	000	1	49	ADD
1	001	1	49	DROP
----	----	----	----	----
1	5FE	16	96	ADD
1	5FF	16	96	DROP
2	000	1	97	ADD
2	001	1	97	DROP
----	----	----	----	----
2	5FE	16	144	ADD
2	5FF	16	144	DROP
3	000	1	145	ADD
3	001	1	145	DROP
----	----	----	----	----
3	5FE	16	192	ADD
3	5FF	16	192	DROP

FIG. 14

10090939-020502

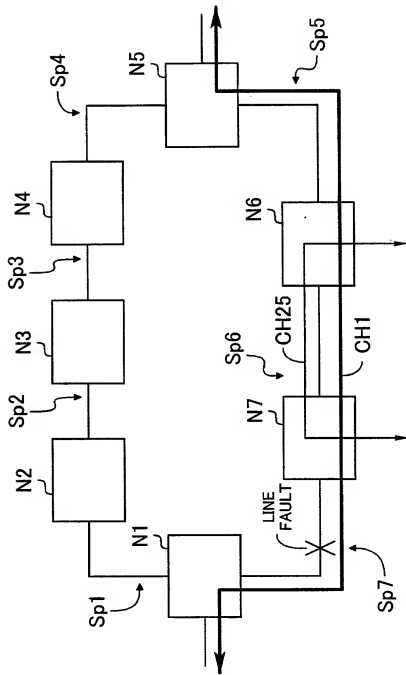


FIG.15

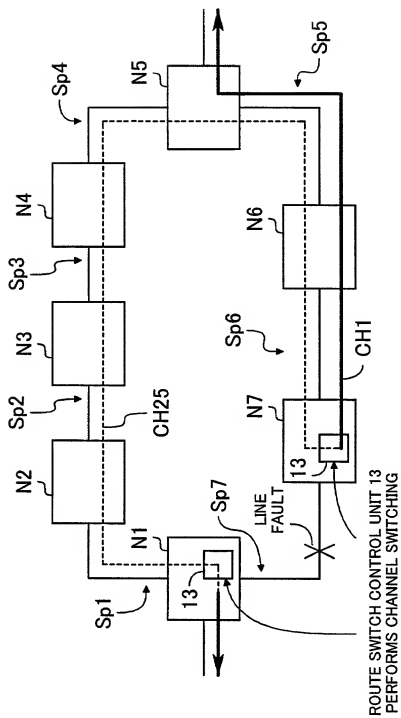


FIG. 16

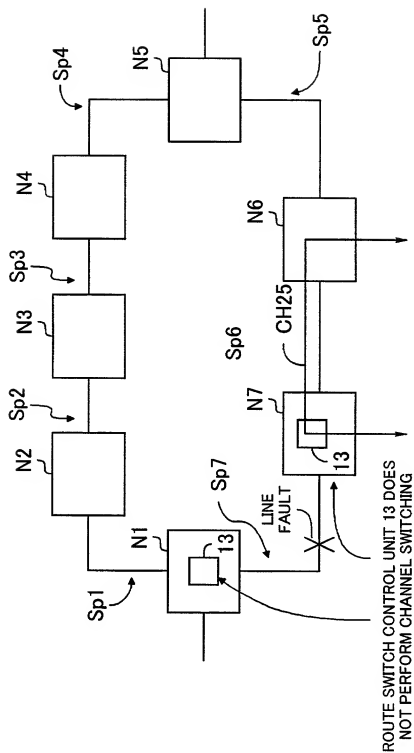


FIG. 17

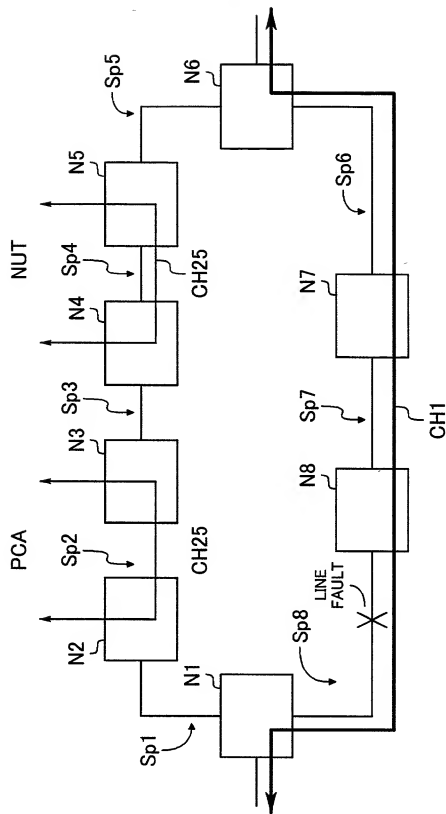


FIG. 18

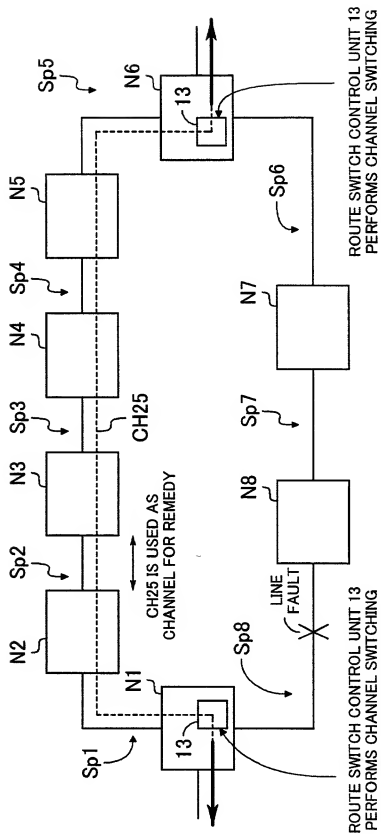


FIG. 19

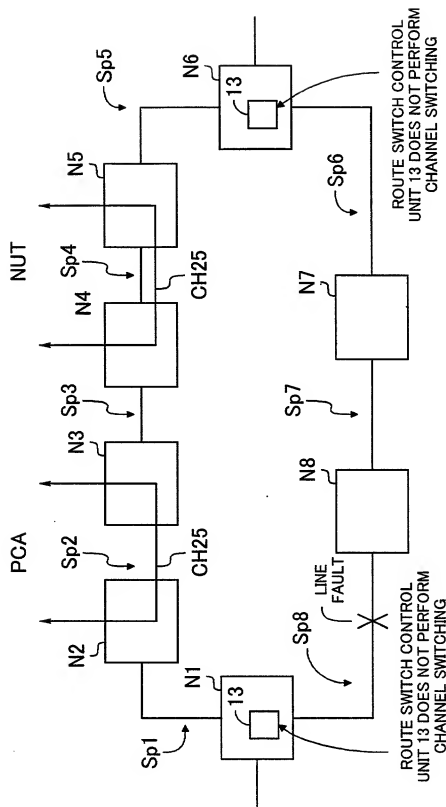


FIG. 20

BASIC NUT

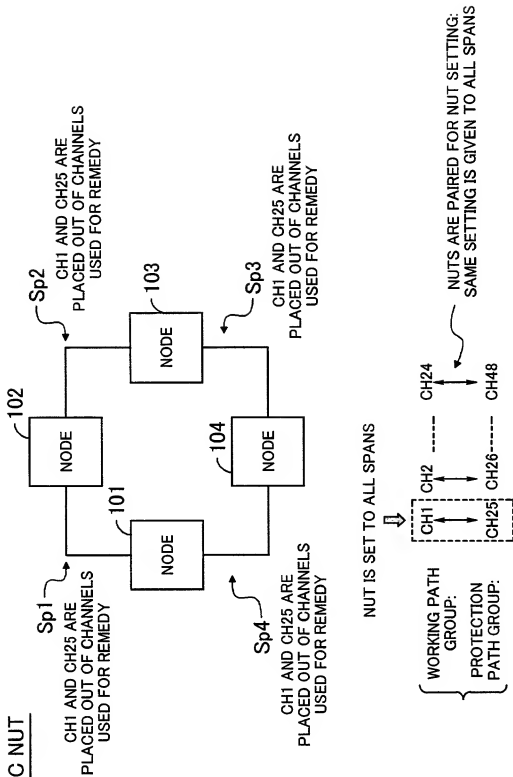


FIG. 21
PRIOR ART

ENHANCED NUT

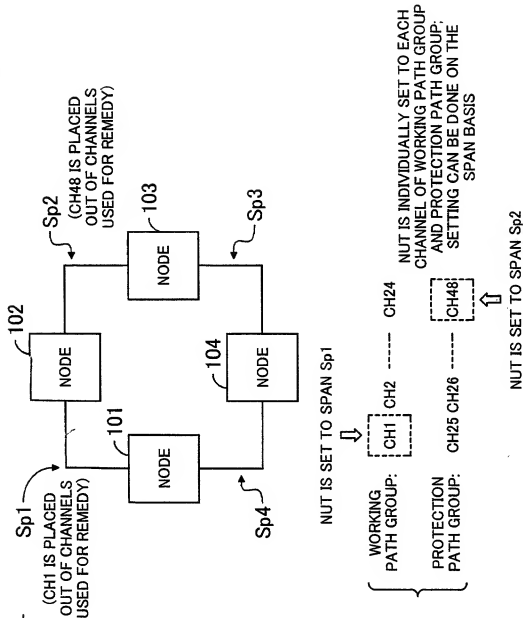


FIG. 22
PRIOR ART